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|  | **NAGARJUNA COLLEGE OF ENGINEERING & TECHNOLOGY**  **(An Autonomous under VTU)**  **DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGG.**  4th Semester 2019-2020  **COURSE HANDOUT** |

**Course Code :** 18ECT42

**Course Title :** Fundamentals of HDL

**Course Teachers : Dr. Rohith S and Dr. Premjyothi Patil**

**Course Co-ordinator : Dr. ROHITH S**

**1. COURSE DESCRIPTION:**

This Course covers the Basic Concepts of Hardware Description Language (HDL) and Programming concepts of Verilog HDL and VHDL. The main topics covered are Operators, data types, Data flow description, behavioral description, structural description, mixed language description and basics of synthesis.

**2. COURSE OBJECTIVE:**

This course will enable students to :

* Understand the basic concept of HDL and to compare between Verilog and VHDL.
* Study the fundamentals of data flow and behavioral designs.
* Understand the concept of structural and mixed language descriptions.
* Apply the concept of task, functions and file processing in HDL.
* Apply the concept of map Register Transfer Logic code to hardware domain.

**3. COURSE PLAN:**

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| **Class Sl No** | **Module and Title / Page No.** | **Topics to be covered** | **% of portions covered** | |
| **Covered in the chapter** | **Cumulative** |
|  | **Module I**  **Introduction**  **T1 Page No.1-36** | Introduction to Hardware Description Language | 20% | 20% |
|  | Why HDL? , |
|  | A Brief History of HDL |
|  | Structure of HDL Module |
|  | Operators |
|  | Data types |
|  | Types of Descriptions |
|  | Types of Description Continued |
|  | simulation and synthesis |
|  | brief comparison of VHDL and Verilog. |
|  | **Module II**  **Data-Flow Descriptions**  **And**  **Behavioral Descriptions**  **T1 Page No.37-47 & Page No 65-91** | Introduction to Data-Flow Model | 20% | 40% |
|  | Highlights of Data-Flow Descriptions |
|  | Structure of Data flow Description |
|  | Data Type – Vectors. |
|  | Introduction to Behavioral model |
|  | Behavioral Description highlights |
|  | Structure of HDL behavioral Description |
|  | Structure of HDL behavioral Description (Programs Continued) |
|  | The VHDL variable: Assignment Statement |
|  | Sequential statements |
|  | Sequential Statements Continued |
|  | **Module III**  **Structural Description**  And  **Mixed-Language Descriptions**  **T1 Page No. 113-118 & Page No 371-403** | Introduction to Structural Description:, | 20% | 60% |
|  | Highlights of structural description |
|  | Programming Concepts |
|  | organization of structural description. |
|  | organization of structural description Continued.. . |
|  | Programming on Structural Description |
|  | Introduction to Mixed-Language Descriptions |
|  | Highlights of Mixed-Language Description |
|  | How to invoke one language from the other |
|  | How to invoke one language from the other Examples |
|  | Limitations of Mixed-Language Description |
|  | **Module IV**  **Procedures, Task and Functions**  **T1 Page No 235-269** | Procedures, Task and Functions | 20% | 80% |
|  | Highlights of Procedures, tasks, and Functions, |
|  | Procedures and tasks |
|  | Programming Examples |
|  | Functions |
|  | Functions Continued…. |
|  | Advanced HDL Description |
|  | File Processing |
|  | Examples of File Processing |
|  | Examples of File Processing Continued.. |
|  | **Module V**  **Synthesis Basics**  **T1 Page No.407-456.** | Introduction to Synthesis | 20% | 100% |
|  | Synthesis Basics |
|  | Highlights of Synthesis |
|  | Synthesis information from Entity and Module |
|  | Examples Synthesis information from Entity and Module |
|  | Continued… |
|  | Mapping Process |
|  | Continued.. |
|  | Mapping Process and always in the Hardware Domain |
|  | Mapping Process and always in the Hardware Domain |

**4. TEXT BOOK:**

**T1.** Nazeih M. Botros: “HDL Programming (VHDL and Verilog)”, (Chapters 1-4,6,8,9,10), Dreamtech Press Publishers, New Delhi, 2008, ISBN-13: 9788177226973

**5. REFERENCE BOOKS:**

**R1**. J. Bhaskar: “A Verilog HDL Primer”, 2nd Edition, BS Publications, Hyderabad, 2001, ISBN: 8178000121.

**R2.** Volnei A. Pedroni: ‘Circuit Design with VHDL”, 1st Edition, Prentice Hall of India Pvt. Ltd., New Delhi, 2004, ISBN: 8120326830.

**6. EVALUATION SCHEME:**

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| --- | --- | --- |
| **Component** | **Weightage** | **Date** |
| CIE 1 | 20% |  |
| CIE 2 | 20% |  |
| Makeup CIE | 20% |  |
| AAT-1 (Open Book Test) | 5% |  |
| AAT 2 (Surprise Test) | 5% |  |
| SEE | 50% |  |

**7. COURSE OUTCOMES:**

On successful completion of this module, students should be able to:

* Describe the various data type, operators and different descriptions in VHDL and Verilog.
* Develop program using data flow and behavioral descriptions in VHDL and Verilog.
* Develop program using structural and mixed language description in VHDL and Verilog.
* Develop program using procedure, task, and functions in VHDL and Verilog.
* Analyze and synthesis VHDL and VERILOG codes for digital circuits.

**Course Teachers HOD**

Dr. Rohith S Dr. Nagesh K N

Dr. PremJyothi Patil