**Course Handout**

General Handout for all courses appended to the time table

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| **Course No. : 19ECI33** | **Dept.: Electronics and Communication Engineering**  |
| **Course Title : Digital Electronic Circuits** | **Semester: IIIrd**  |
| **Instructor-in-charge : Ms. Jyothi** [**jyothisk53@ncetmail.com**](jyothisk53%40ncetmail.com) | **Academic Year: 2020-21** |
| **Lab. Instructor : Ms. Jyothi** | **Date**: 03/08/2020 |

**Subject Description:**

This Course covers the fundamentals of switching theory to the solution of logic design problems. This means that the students will learn both the basic theory of switching circuits and how to apply it. After a brief introduction, the students will study Boolean algebra, which is the basic mathematical tool needed to analyze and synthesize an important class of switching circuits. Starting from a problem statement, the students will learn to design circuits of logic gates that have a specified relationship between signals at the input and output terminals. Then the students will study the logical properties of flip-flops, which serve as memory devices in sequential switching circuits. By combining flip-flops with circuits of logic gates, the students will learn to design counters, adders, sequence detectors, and similar circuits. The purpose of this course is to develop the strong fundamentals in Logic Design and to apply switching theory to the solution of logic design problems.

**Text Books:**

**T1.** John M Yarbrough: “Digital Logic Applications and Design”, 3rd Edition, Cengage Learning, New Delhi, Reprint, 2012, ISBN-13: 978-81-315-0058-3, ISBN-10: 81315-0058-6.

**T2.** Donald D Givone: “Digital Principles and Design”, 1st Edition, Tata McGraw Hill, New Delhi, Reprint, 2005, ISBN: 0-07-052906-X.

**REFERENCE BOOKS:**

**R1**. Charles H Roth: “Fundamentals of logic design”, 5th Edition, Thomson, New Delhi, Reprint, 2007, ISBN: 81-315-0043-8.

**R2.** M. Morris Mano and Charles R. Kime: “Logic and computer design Fundamen- tals”, 2nd Edition, Pearson, Reprint, 2005, ISBN: 81-7808-334-5.

**PREREQUISITES:**

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| --- | --- | --- |
| 1. Basic concepts of number system
2. Basic knowledge of electronic circuits
 | Self-study | RemarksStudents have completed this Courses.  |

**LECTURE PLAN:**

|  |  |  |  |
| --- | --- | --- | --- |
| **Topic** | **Topic Details** | **Number****of****Lectures** | **Unit/ Chapter****Reference** |
| **Module – I****Simplification of Boolean functions****T1 page no****84 - 129** | Definition of combinational logic | 1 | T1 3.1 |
| Canonical forms | 2 | T1 3.2 |
| Generation of switching equations from truth tables | 3 | T1 3.3 |
| Karnaugh maps-three, four | 4 | T1 3.4.1 |
| Incompletely specified functions (Don’t Care terms) | 5 | T1 3.4.2 |
| Simplifying Max term equations, | 6 | T1 3.5 |
| QuineMc-Clusky minimization technique | 7 | T1 3.6 |
| Map entered variable | 8 | T1 3.7 |
| **Module – II****Combinational Logic Circuits****T2 page no****231 - 266** | Parallel adder | 9 | T2 5.1 |
| Parallel subtractor | 10 | T2 5.1.1 |
| carry look ahead adder | 11 | T2 5.1.2 |
| Magnitude Comparator | 12 | T2 5.3 |
| Decoders  | 13 | T2 5.4 |
| Encoders | 14 | T2 5.5 |
| Multiplexers | 15 | T2 5.6 |
| Logic Design with Multiplexers | 16 | T2 5.6.1 |
| **Revision** |  |  |  |
| **AAT 1** |  |  |  |
| **Module – III****Flip-Flops and Simple Flip –Flops Applications****T2 page no** **302 - 324** | Basic Bistable Element, Latches, SR Latch | 17 | T2 6.1,6.2 |
| Application of SR Latch, A Switch Debouncer | 18 | T2 6.2.2 |
| gated SR Latch, The gated D Latch | 19 | T2 6.2.4 |
| Master-Slave SR Flip-Flops | 20 | T2 6.4.1 |
| The Master-Slave JK Flip-Flop | 21 | T2 6.4.2 |
| 0’s and 1’s Catching | 22 | T2 6.4.3 |
| Edge Triggered D Flip-Flop | 23 | T2 6.5 |
| Negative-Edge Triggered D Flip-Flop | 24 | T2 6.5.2 |
| **Module – IV****Sequential Circuits****T2 page no****329 - 352****R1 page no****342 - 348** | Characteristic Equations | 25 | T2 6.6 |
| Registers | 26 | T2 6.7 |
| Counters - Binary Ripple Counters | 27 | T2 6.8.1 |
| Synchronous Binary counters | 28 | T2 6.8.2 |
| Counters based on Shift Registers | 29 | T2 6.8.3 |
| Design of a Synchronous counters | 30 | T2 6.9 |
| Design of a Synchronous Mod-N Counter using clocked JK and D Flip-Flop | 31 | T2 6.9.1 |
| Design of a Synchronous Mod-N Counter using clocked T Flip-Flops | 32 | T2 6.9.2 |
| **Revision**  |  |  |  |
| **AAT2** |  |  |  |
| **Module – V****Sequential Design****T1 page no****322 - 349** | Introduction, Mealy and Moore Models | 33 | T1 8.1 |
| State Machine Notation | 34 | T1 8.2 |
| Present state, Next state, State diagram, State Table | 35 | T1 8.2.1 |
| Excitation table and Equations, Excitation Realization Cost | 36 | T1 8.2.2 |
| Synchronous Sequential Circuit Analysis | 37 | T1 8.3 |
| Analysis Principles and Examples | 38 | T1 8.4 |
| Construction of state diagram | 39 | T1 8.5 |
| Examples of construction of state diagram | 40 | T1 8.5.1 |

Evaluation Scheme:

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| --- | --- | --- | --- |
| **Component** | **Duration** | **Weightage** | **Date (Time)** |
| **CIE 1** | 60 min | 10% | 29/9/2020 |
| **CIE 2** | 60 min | 10% | 07/11/2020 |
| **AAT 1** | 2 days | 2.5% | 29/9/2020(Tentative) |
| **AAT 2** | 2 days | 2.5% | 07/11/2020(Tentative) |
| **Make up CIE** | 90 min |  | 26/11/2020 |
| **Practical Lab Exam** | 120 min | 25% | 28/11/2020(Tentative) |
| **SEE** | 180 min | 50% | 14/12/2020(Tentative) |
| **Make up SEE** | 180 min |  | 16/01/2021(Tentative) |
| **Total** |  | 100% |  |

**Notices:** All notices will be displayed on NCET and in Department website.

**Chamber Consultation Hour:** Wednesday 2:00Pm to 4:00 Pm

**Makeup Policy:** To be granted only in case of serious illness or emergency.

**Email Policy:** Communication through email. If you want to discuss anything, you are most welcome to meet me during chamber consultation hours or immediately after the class. Academic queries/doubts can be posted in Moodle.

Ms. Jyothi

**Course-in-charge**